Optically Isolated Probes for Modern Power Electronics

Application Note

1. Introduction

Wide-bandgap semiconductor technologies such as SiC and GaN are rapidly transforming modern power electronics. Faster switching transitions, higher bus voltages, and increased power density enable more efficient and compact systems. However, these same characteristics introduce significant measurement challenges.

High dv/dt transitions often exceeding tens or hundreds of kV/μs generate strong common-mode transients and displacement currents. These effects directly stress the measurement system and can distort observed waveforms, especially when measuring high-side nodes or fast gate transitions.

In modern converter development, accurate measurement of gate-to-source voltage (VGS) is critical. Misinterpreting overshoot, ringing, or switching speed can lead to:

- Incorrect device characterization
- Suboptimal gate resistor selection
- Underestimated EMI performance
- Reduced long-term reliability

To address these challenges, probe architecture plays a decisive role. This application note compares a traditional high-voltage differential probe with an optically isolated probe in a controlled switching environment, highlighting why optical isolation becomes essential in modern high-voltage designs.

2. Theoretical Background: CMRR and CMTI

2.1 Common-Mode Rejection Ratio (CMRR)

CMRR describes the ability of a probe to reject common-mode voltage while accurately measuring differential voltage.

$$CMRR = 20\log\left(\frac{A_d}{A_{cm}}\right)$$

In practical systems:

- CMRR decreases with frequency
- Fast switching edges contain high-frequency components
- Small input mismatches create differential error

At high dv/dt, degraded CMRR results in artificial ringing, overshoot, and waveform distortion.

2.2 Common-Mode Transient Immunity (CMTI)

CMTI defines the probe's tolerance to rapid voltage transitions.

$$V_{error} \propto \frac{dv}{dt} \times C_{parasitic}$$

In differential probes, parasitic capacitances allow displacement current to couple into the measurement path. Optical isolation removes the conductive ground path, significantly improving immunity to common-mode transients.

3. Test Configuration

3.1 Measurement Equipment

The evaluation was performed using:

- Rigol DHO5108 Oscilloscope
- Rigol PIA1100 Optically Isolated Probe
- Rigol RP1100D Differential Probe
- High-voltage MOSFET switching board

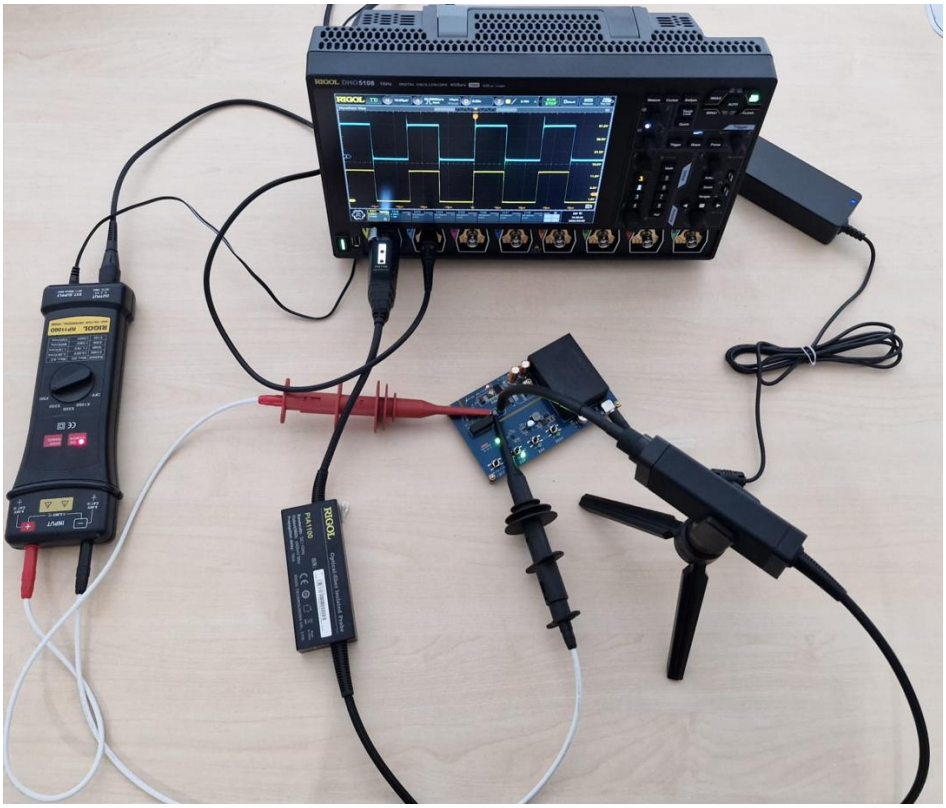

Figure 1. Complete laboratory setup including DHO5108 oscilloscope, PIA1100 optically isolated probe, RP1100D differential probe, and high-voltage MOSFET test board.

3.2 Test Board Description

The high-voltage board consists of MOSFET transistors configured in a switching topology. Two measurement nodes were evaluated:

- L-GS (Low-side gate-to-source voltage)
- H-GS (High-side gate-to-source voltage)

Selectable bus voltages:

- 20 V
- 80 V
- 300 V

Figure 2. High-voltage MOSFET switching board with selectable bus voltage levels.

3.3 Probe Connection Detail

Both probes were connected sequentially to identical test points. Connection geometry and grounding were kept consistent to ensure fair comparison.

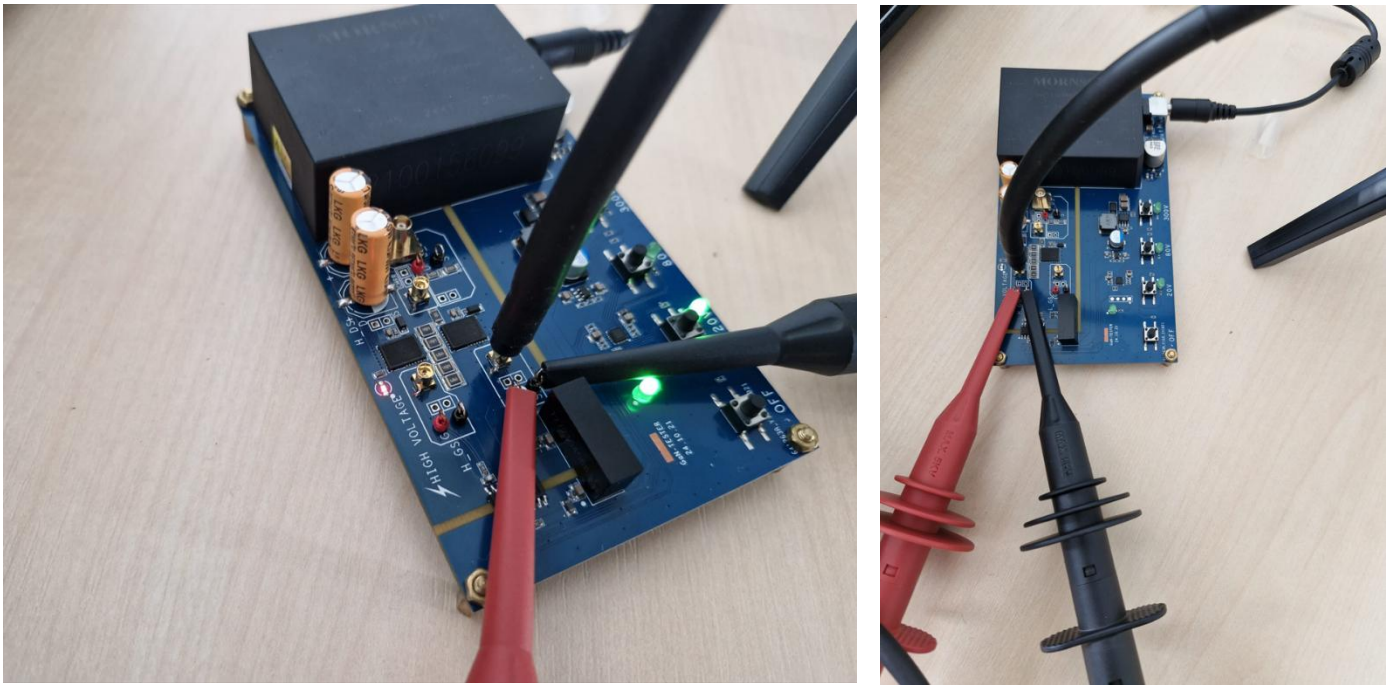

Figure 3. Close-up view of probe connections to the gate-to-source measurement nodes.

4. Low-Side Gate (L-GS) Measurements

4.1 L-GS at 20 V

Even at a relatively low bus voltage of 20 V, a measurable difference between probe architectures is already observable.

Although the DC bus level is moderate, the gate transitions remain fast. These rapid edges generate sufficient dv/dt stress to expose limitations in high-frequency common-mode rejection.

Before analyzing edge detail, it is instructive to examine the full multi-cycle switching behavior.

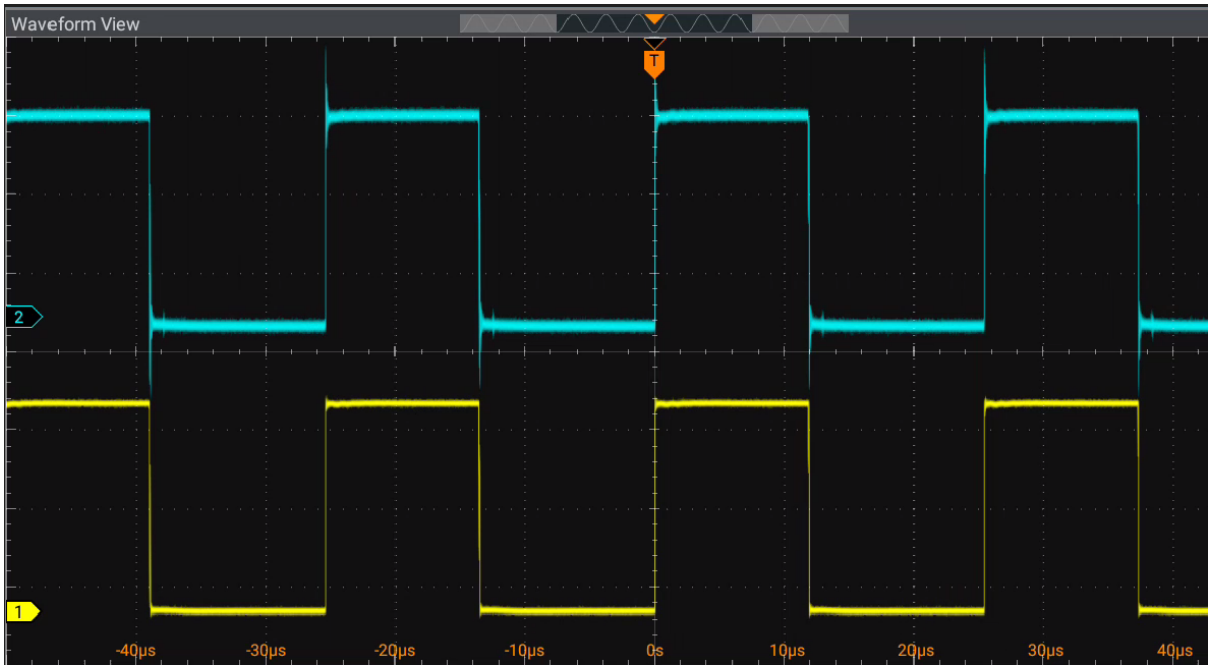

Figure 4. Full low-side gate waveform at 20 V bus voltage. The differential probe exhibits increased baseline noise compared to the optically isolated probe.

Across several switching periods, the optically isolated probe maintains a stable baseline and consistent amplitude. The waveform remains clean, and the ringing behavior corresponds closely to expected circuit parasitics.

In contrast, the differential probe exhibits additional high-frequency noise superimposed on both the high and low states. This noise is not part of the actual circuit response but results from limited high-frequency CMRR and parasitic coupling within the probe structure.

Even at 20 V, dv/dt not bus magnitude is the dominant stress mechanism affecting measurement integrity.

4.2 L-GS Zoomed Transitions – Voltage Escalation

4.2.1 Zoom – 20 V

Figure 5. Zoomed L-GS transition at 20 V bus voltage.

At 20 V, the differential probe already exhibits elevated high-frequency noise components on the switching edge. The optically isolated probe maintains improved edge clarity and lower superimposed disturbance.

This demonstrates that dv/dt not only bus magnitude determines measurement stress.

4.2.2 Zoom – 80 V

Figure 6. Zoomed L-GS transition at 80 V bus voltage.

At 80 V, the effect of increasing dv/dt becomes more pronounced. The differential probe shows increased oscillatory behavior and amplified ringing amplitude. The optical probe maintains more controlled waveform definition with reduced apparent noise contribution.

Common-mode conversion error increases with voltage transition amplitude.

4.2.3 Zoom – 300 V

Figure 7. Zoomed L-GS transition at 300 V bus voltage under high dv/dt stress.

At 300 V, the measurement environment reaches high common-mode transient stress. The differential probe exhibits substantial ringing amplification and visible distortion.

The optically isolated probe maintains superior edge fidelity and reduced superimposed disturbance, clearly demonstrating improved CMTI performance.

At this voltage level, probe architecture becomes a dominant factor in waveform accuracy.

5. High-Side Gate (H-GS) Measurements

High-side gate measurement represents a more demanding scenario than low-side measurement.
Although the DC bus voltage is 20 V, the source node of the high-side MOSFET is dynamically moving with the switching waveform. This creates significant common-mode movement relative to oscilloscope ground.

Because the reference potential is floating, probe architecture plays a critical role in maintaining waveform integrity.

5.1 H-GS – Full Signal Overview

Before analyzing edge transitions, the full multi-cycle waveform is evaluated.

Figure 8. Full high-side gate waveform at 20 V bus voltage.

Across multiple switching cycles, the optically isolated probe maintains:

- Stable high-level amplitude
- Clean low-state baseline
- Consistent cycle-to-cycle behavior

The differential probe, however, shows:

- Increased high-frequency disturbance on both high and low states
- Elevated ringing during transitions
- Slight baseline instability between switching periods

This indicates that even at 20 V, floating-node measurement conditions amplify common-mode coupling effects inside the differential probe structure.

5.2 H-GS – Rising Edge (20 V)

To better understand the transition behavior, the rising edge is examined in detail.

Figure 9. Zoomed high-side gate rising transition at 20 V.

During the rising transition:

- The differential probe exhibits amplified ringing immediately after the edge.
- High-frequency oscillations are visibly stronger and persist longer.
- Additional superimposed noise appears on the settling portion of the waveform.

The optically isolated probe presents:

- Cleaner transition shape
- Reduced high-frequency amplification
- More controlled settling behavior

This difference is consistent with improved CMTI performance and reduced parasitic common-mode coupling.

5.3 H-GS – Falling Transition

The falling edge further highlights the probe architecture differences.

Figure 10. High-side gate falling transition at 20 V.

During the falling transition:

- The differential probe shows pronounced oscillatory behavior immediately after the edge.
- Ringing amplitude is visibly higher.
- Additional transient spikes appear that are not consistent with the expected gate-drive response.

The optically isolated probe maintains:

- Improved edge clarity
- Reduced overshoot
- Faster stabilization after transition

This confirms that floating high-side nodes magnify common-mode stress, and optical isolation significantly improves measurement fidelity under these conditions.

6. Conclusion

This evaluation compared a traditional differential probe with an optically isolated probe during low-side and high-side MOSFET gate measurements under increasing bus voltage conditions.

The results demonstrate that probe-related measurement differences appear even at 20 V and become progressively more pronounced at 80 V and 300 V. As dv/dt increases, the differential probe exhibits elevated high-frequency noise, amplified ringing, and greater baseline disturbance. These effects are driven by limited high-frequency CMRR and sensitivity to common-mode transients.

In contrast, the optically isolated probe consistently maintains improved waveform clarity, reduced superimposed noise, and more stable multi-cycle behavior. High-side measurements, where the reference node is dynamically moving, further highlight the benefit of galvanic isolation in minimizing common-mode coupling effects.

These findings confirm that in modern fast-switching power electronics systems, measurement accuracy is strongly influenced by probe architecture. Optically isolated probes provide enhanced CMTI performance and improved signal fidelity, enabling more reliable analysis of switching behavior in high dv/dt environments.

In high-speed power electronics, measurement integrity is determined not only by the oscilloscope, but by the probe architecture that connects the instrument to the circuit.

Related Literature

The following documents and resources provide additional information related to the instruments and measurement techniques discussed in this application note:

- Rigol Technologies, *DHO5000 Series High-Resolution Oscilloscope Datasheet*.
- Rigol Technologies, *PIA1100 Optically Isolated Probe Datasheet*.
- Rigol Technologies, *RP1100D High-Voltage Differential Probe Datasheet*.
- Texas Instruments, *Understanding Common-Mode Rejection Ratio (CMRR)*, Application Report.
- Analog Devices, *Common-Mode Transient Immunity in High-Speed Systems*, Technical Article.
- IEEE, *Measurement Techniques for High dv/dt Power Electronics Systems*, Conference Proceedings.

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